REMARKS

Prior to the present amendment, claims 1-2, 4-6, 8-9, and 11-13 were pending in the present application. By this amendment, Applicant has amended claims 1, 6, 8, and 13, and has canceled claims 2 and 9. Thus, claims 1, 4-6, 8, and 11-13 remain in the present application. Reconsideration and allowance of pending claims 1, 4-6, 8, and 11-13 in view of the above amendments and the following remarks are respectfully requested.

The Examiner has rejected claims 1-2, 4-6, 8-9, and 11-13 under 35 USC §103(a) as being unpatentable over U.S. Patent No. 6,563,183 to En et al (hereinafter "En") in combination with U.S. Patent Publication No. 2005/0048765 to Kim (hereinafter "Kim"). Applicant respectfully submits that the present invention, as defined by amended independent claims 1 and 8, is patentably distinguishable over En and Kim, either singly or in combination.

En is directed to a gate array with multiple dielectric properties. According to En, an integrated circuit is fabricated on a semiconductor substrate, including first and second field effect transistors. The first field effect transistor includes a first polysilicon gate positioned above a first channel region of the substrate and isolated from the first channel region by a first dielectric layer extending the entire length of the first polysilicon gate. The first dielectric layer includes a first dielectric material with a first dielectric constant. The second field effect transistor consists of a second polysilicon gate positioned above a second channel region on the substrate and isolated from the second channel region by a

second dielectric layer extending the entire length of the second polysilicon gate. The second dielectric layer has a second dielectric material with a second dielectric constant. The first dielectric constant and the second dielectric constant may be different. See the flow chart of Figure 2, and Figures 5a through 5i and their related descriptions in En.

According to En, utilization of different dielectrics with different dielectric constants results in a gate array that can include smaller, faster transistors having a high dielectric constant, with additional flexibility in that transistors with different operating properties can be fabricated and used. See, column 10, lines 13-21 of En.

However, En is not directed to formation of a thin, high quality buffer layer utilizing a silicon tetrachloride precursor in a field effect transistor in order to prevent the problems associated with transistor gates having low quality, non-uniform, thick, lower-k, and pin-holed dielectrics which in turn result from randomly and unintendedly grown thermal oxide at the silicon/high k interface in the gate of the transistor. See, for example, page 8, line 20 through page 9, line 9 of the present application. Moreover, the invention teaches use of aluminum oxide, which is specifically suitable for use as a high-k dielectric over an ALD silicon oxide layer and in the gate of a transistor.

Thus, the present invention discloses and claims "utilizing a silicon tetrachloride precursor in an atomic layer deposition process to form a buffer layer" on the substrate and "forming a high-k dielectric layer over [the] buffer layer, [the] high-k dielectric layer comprising aluminum oxide"; and thereafter "forming a gate electrode layer over [the] high-k dielectric layer." In addition to the fact that En does not address the problems

addressed by the present invention, En does not disclose or suggest, for example, use of silicon tetrachloride precursor, nor use of aluminum oxide as a high-k dielectric. Moreover, En does not disclose or suggest use of an ALD silicon oxide buffer layer formed with silicon tetrachloride precursor and an overlying high-k dielectric layer formed with aluminum oxide as parts of a gate of a transistor. As such, the present invention, as defined by the amended claims, is patentably distinguishable over En.

The Examiner has cited U.S. Patent Publication No. 2005/0048765 to Kim (hereinafter "Kim") as disclosing use of silicon tetrachloride to form oxide in an ALD process. However, Kim is directed to sealing pores in a *low-k dielectric* damascene process for forming conductive layers. See, for example, Figure 3A of Kim and its related description. As such, Kim specifically teaches away from use of an ALD layer in conjunction with *high-k dielectrics*. For example, Kim does not disclose or suggest "forming a high-k dielectric layer over [the] buffer layer, [the] high-k dielectric layer comprising aluminum oxide." Moreover, Kim is not directed to fabrication of a field effect transistor or its gate, but to the formation of conductive patterns in a damascene process. In contrast, the invention discloses and claims "forming a gate electrode layer over [the] high-k dielectric layer."

The Examiner has stated that Kim is cited for suggesting that an ALD layer formed with silicon tetrachloride precursor can be used in a transistor utilizing a high-k gate dielectric. However, there is no suggestion whatsoever in Kim for such a departure from the teachings of Kim, where Kim in fact discloses sealing pores in a *low-k dielectric*

damascene process. Moreover, Kim is not directed to formation of transistor gates, but to patterning conductors. It is noted that Applicant has not claimed that the invention has for the first time utilized an ALD layer, nor that the invention has for the first time utilized a high-k dielectric. Likewise, Applicant has not claimed that the invention is about forming an ALD layer with silicon tetrachloride precursor. Applicant has merely claimed that the combination of an ALD buffer layer formed with silicon tetrachloride precursor, and a high-k dielectric formed with aluminum oxide, both in the gate of a field effect transistor, is novel and inventive. It is submitted that Kim does not provide suggestions or teachings to cure the deficiencies of En. In other words, the general proposition that an ALD layer can be formed with silicon tetrachloride precursor does not suggest or overcome the deficiencies of En discussed above.

For all the foregoing reasons, Applicant submits that claims 1, 4-6, 8, and 11-13 remaining in the present application are patentably distinguishable over En and Kim, either singly or in combination. As such, an early notice of allowance directed to pending claims 1, 4-6, 8, and 11-13 is respectfully requested.

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Respectfully Submitted,
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